

Press release

Target Compiler Technologies sees strong growth for its application-specific processor design tools in Japanese market

Yokohama, January 24, 2008 – At the start of the Electronic Design and Solutions Fair in Yokohama today, Belgian EDA vendor Target Compiler Technologies said that its tools for the design of application-specific processors (ASIPs) are enjoying an increasingly strong adoption by the Japanese electronics industry. Target's "IP Designer" tool suite (formerly "Chess/Checkers") is especially being used by system-on-chip (SoC) design groups, in the context of advanced multi-media and wireless system designs.

"Our ASIP design tools were introduced in Japan more than three years ago," commented Jeroen De Lille, Target's Vice President of Sales and Marketing. "Since then, the adoption of our tools has been on a steady growth path. 2007 has been a good year, as several large Japanese electronic companies were added to our customer list. 2007 also marked the introduction of first end products in the Japanese market that are powered by ASIPs designed with our tools, notably in cell phones," De Lille added.

Traditional SoC designs contain a combination of general-purpose processor cores and hardwired, fixed-function blocks. Next-generation SoCs call for more diversity in terms of system functionality and supported standards. This evolution has fuelled a trend to replace such hardwired blocks by more programmable architectures, without however giving up on computational performance and low power dissipation. Such a combination of features is obtained by using ASIPs, which are programmable blocks that support architectural specialisation and significantly more parallelism than conventional processors.

"We consider ASIPs as an ideal solution to meet the performance, power, and flexibility requirements of our next-generation chips," said Shohei Okamura, General Manager of OLYMPUS DIGITAL SYSTEM DESIGN CORP. (ODS). "We had an important need for efficient EDA tools to design such ASIPs fast and reliably. We knew of Target's track record in this segment of the EDA market, so it was a logical choice to engage with them," Okamura continued.

ODS is using the IP Designer tool suite both for architectural exploration of its new ASIPs, for generating efficient low-power register-transfer level (RTL) implementations of these ASIPs, and for building complete software development kits to program the ASIPs from C source code.

"We have especially been impressed with Target's optimising C compiler technology for ASIPs," said Takashi Hirano, Senior Engineer at ODS. "Target's C compiler can efficiently exploit the vector processing capabilities, the instruction-level parallelism, and the special addressing modes of our ASIP architectures. This makes it easy to program multiple algorithmic standards on our ASIPs using a high-level language like C, while obtaining an execution speed and code density comparable to manually optimised assembly code," Hirano added.

"We are extremely pleased that ODS selected Target as its EDA partner for ASIP design in its next-generation SoCs," said Gert Goossens, CEO of Target. "This move by such an important player in the multimedia and graphics market confirms the growing acceptance of the ASIP paradigm in SoC design, and strengthens Target's position as a leading tool vendor in this space."

Target is represented in Japan by Innotech Corporation. "In recent years, Electronic System-Level tools have gained a prominent position in Innotech's portfolio of EDA tools," said Takashi Takahashi, Director and General Manager of IC Solution Business Group of Innotech. "The Japanese market for ESL tools is growing tremendously, and we are happy to have Target's IP Designer tool suite as one of our successful ESL products," Takahashi added.

About OLYMPUS DIGITAL SYSTEM DESIGN CORP.

OLYMPUS DIGITAL SYSTEM DESIGN CORP. (ODS) performs advanced SoC (LSI) design and research and development of digital systems in the Olympus group. ODS develops SoCs and application software optimised for advanced SoCs through the coherent development from algorithm examination to LSI implementation and evaluation. By hardware-software co-design based on a wide LSI development experience, ODS realises a speed-up of its development and contributes to differentiation in the digital signal processing area, for practical application in various Olympus products.

About Target Compiler Technologies

Target Compiler Technologies is the leading provider of software tools to automate the design, programming and verification of application-specific processor cores (ASIPs). Target's "IP Designer" tool suite has been applied by customers worldwide for diverse application domains, including GSM, WCDMA and HSDPA handsets, VoIP, audio coding, car infotainment, ADSL and VDSL modems, wireless LAN, hearing instruments, mobile image processing, video processing, and various control and interfacing applications. Target is a spin-off of IMEC, is headquartered in Leuven, Belgium, with North American operations in Boulder, Colorado. For more information about Target Compiler Technologies, visit www.retarget.com.

About Innotech Corporation

Founded in 1987, Innotech is Japan's premier importer of high-end semiconductor devices, EDA software and equipment, and a skilled support partner to many of Japan's top electronics makers. The company maintains direct relationships with every major semiconductor manufacturer, electronics company, and other leading suppliers in Japan. Today's Innotech is a high-paced company that prides itself on making swift but informed decisions to keep up with the pace of an ever-changing electronics market. As an importer, the company leverages deep relationships with some of North America's, Europe's, and Asia's suppliers of most advanced electronics components, EDA software, and semiconductor devices. For more information, visit www.innotech.co.jp.

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